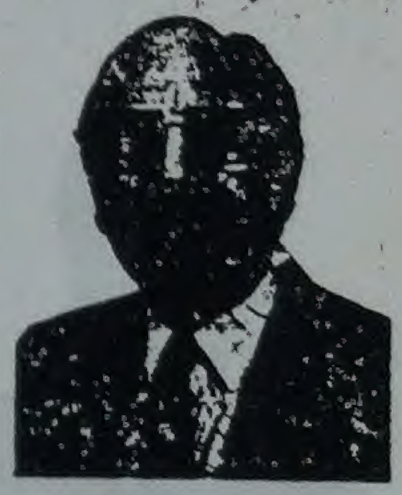
MISC. DOCS - K. BUCKLE

PASSPORT



الاسم حسن علي ابراهيم علي حسن

Nom Hassan Ali Ibrahim Ali

مكان الميلاد الدخلية

Lieu de Naissance Dakhlia

تاريخ الميلاد يوم ٢١ من شهر ١١ سنة ١٩٢٨

Date de Naissance 21 11 1928

المهنة أو الوظيفة مدير عام وصاحب مصنع سيليكو

Profession Managing Director & Owner Silico G.

الأوصاف المميزة لا شيء

Signes Particuliers Nil

العنوان ق ج م ع ١٢٧ شارع عمر بن الخطاب مصر الجديدة

لون العينين بني

Couleur des Yeux Brown

الطول ١٧٥ سم

Taille 175 cm

PASSPORT

Photographie

اسم الزوجة

مكان الميلاد

تاريخ الميلاد يوم من شهر سنة

المهنة أو الوظيفة

NOM De L'épouse

Lieu de Naissance

Date de Naissance

Profession

Taille الطول

Couleur des Yeux لون العينين

Signes Particuliers الأوصاف المميزة

FOR TOM

FROM SALLY -

Photographie	
اسم الزوجة	لون العينين .....
مكان الميلاد	Couleur des Yeux .....
تاريخ الميلاد في يوم ..... من شهر ..... سنة	الطول .....
المهنة أو الوظيفة	Taille .....
NOM De L'épouse	.....
Lieu de Naissance	.....
Date de Naissance	.....
Profession	.....
Taille ..... الطول	.....
Couleur des Yeux ..... لون العينين	.....
Signes Particuliers ..... الأوصاف المميزة	.....

FOR TOM

FROM SALLY -

جمهورية مصر العربية
وزارة الداخلية
مصلحة وثائق السفر والهجرة والجنسية

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RÉPUBLIQUE ARABE D'EGYPTE
MINISTÈRE DE L'INTÉRIEUR
ADMINISTRATION DES PASSEPORTS,
DE L'IMMIGRATION ET
DE LA NATIONALITÉ.

Le Ministre des Affaires Etrangères Prie les autorités concernées de Laisser Passer Le porteur de ce passeport et de lui porter L'aide et La protection Le cas echéant

جواز سفر

رقم الجواز ٨٨٠٩٧

الجهة التى أصدرته ..... بون

فى يوم ..... ١٠ ..... من شهر ..... ١٠ ..... سنة ١٩٨٨

تنتهى صلاحية هذا الجواز .....

فى يوم ..... ٩ ..... من شهر ..... ١٠ ..... سنة ١٩٨٩

N° du Passeport 88097

Fait à Bonn Le ..10.. du mois de ..10.. 19 88

Il Expire Le 9.10.1989

~~Le Directeur Général~~

Ou Le Consul Général

~~مدير المصلحة~~

أو القنصل العام

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جمهورية مصر العربية
وزارة الداخلية
مصلحة وثائق السفر والهجرة والجنسية

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جواز سفر رقم ٨٨٠٩٧

الجهة التي أصدرته بون

في يوم ١٠ من شهر ١٠ سنة ١٩٨٨

تنتهي صلاحية هذا الجواز

في يوم ٩ من شهر ١٠ سنة ١٩٨٩

N° du Passeport 88097

Fait à Bonn Le 10 du mois de 10 19 88

Il Expire Le 9.10.1989

المدير العام

Le Directeur Général

Ou Le Consul Général

ROBERT F. BICKEL & ASSOCIATES
Engineering & Technical Consultants

Oil & Gas
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Systems Documentation

2700 Post Oak Blvd., Ste. 2450
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dsw

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1500 West Hampden
Hampden West Park Bldg. 4C

Telephone (303) 762-8001 FAX (303) 762-8004

FAX Message
1 OF 12

TO: Bob Bickel 363-7394

Company: _____

FAX No Called: 371-8022

Date: 13 DEC 90

MESSAGE

Dear Bob;

Here are the data sheets on the Harris version. If I can be of further assistance, please call.

Sincerely,

LEO A. RUEUP

1 Attch: Data sheets for CA3318 (TS8308)

HARRIS SEMICONDUCTOR
HARRIS RCA · GE · INTERSIL

PRELIMINARY
Subject to Change

CA3318C
CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

GENERAL DESCRIPTION

The Harris CA3318C is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3318 operates over a wide full-scale input-voltage range of 4V up to 7.5V with maximum power consumptions depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15 MHz, the typical power consumption of the CA3318 is 150 mW.

The intrinsic high conversion rate makes the CA3318 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3318's in series to increase the resolution of the conversion system. A series connection of two CA3318's may be used to produce a 9-bit high-speed converter. Operation of two CA3318's in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz).

256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3318.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

FEATURES

- CMOS Low Power with 30S Speed (150 mW Typ.)
- Parallel Conversion Technique
- 15-MHz Sampling Rate (67 ns Conversion Time)
- 8-Bit Latched 3-State Output with Overflow Bit
- ±1 LSB Accuracy (Typ.)
- Single Supply Voltage (4 to 7.5V)
- 2 Units in Series Allow 9-Bit Output
- 2 Units in Parallel Allow 30 MHz Sampling Rate

APPLICATIONS

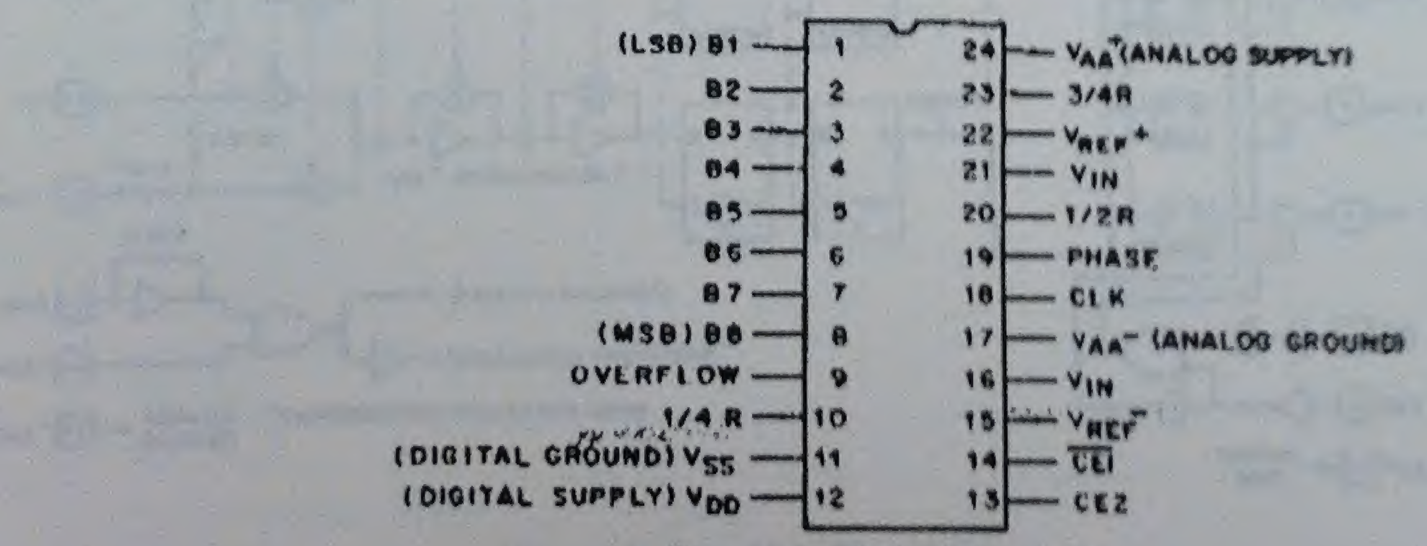
- TV Video Digitizing (Industrial/Security/Broadcast)
- High-Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High-Energy Physics Research
- High-Speed Oscilloscope Storage/Display
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- µP Data Acquisition Systems

ORDERING INFORMATION

Part Number	Linearity (INL)	Sampling Rate	Temperature Range	Package
CA3318CE	±1.5 LSB	15 MHz (67 ns)	−40°C to +85°C	24 Pin Plastic DIP
CA3318CD	±1.5 LSB	10 MHz (100 ns)	−40°C to +85°C	24 Pin Ceramic DIP

NOTE: Consult sales office for availability of SOIC package.

Top View



0194-1

Figure 1: Pin Configuration

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range (V_{DD} or V_{AA}^+)
(Referenced to V_{SS} or V_{AA}^- Terminal, Whichever is More Negative) ..... −0.5V to +8V

Input Voltage Range
CE2 and $\overline{CE1}$ ..... V_{AA}^- − 0.5V to V_{DD} +0.5V
Clock, Phase, V_{REF}^-,
½ Ref ..... V_{AA}^- − 0.5V to V_{AA}^+ + 0.5V
¼ Ref ..... V_{SS} − 0.5V to V_{DD} + 0.5V
V_{IN}, ¾ REF, V_{REF}^+ ..... V_{AA}^- − 0.5V to V_{AA}^- +7.5V

Output Voltage Range
Bits 1-8, Overflow
(Outputs Off) ..... V_{SS} − 0.5V to V_{DD} + 0.5V

DC Input Current ..... ±20 mA
Clock, Phase, $\overline{CE1}$, CE2, V_{IN}, Bits 1-8, Overflow

Power Dissipation per Package (P_D)
For T_A = −40°C to +55°C ..... 315 mW
For T_A = 55°C to 85°C ..... Derate Linearly at 3.3 mW/°C

Temperature Range
Operating ..... −40°C to +85°C
Storage ..... −65°C to +150°C

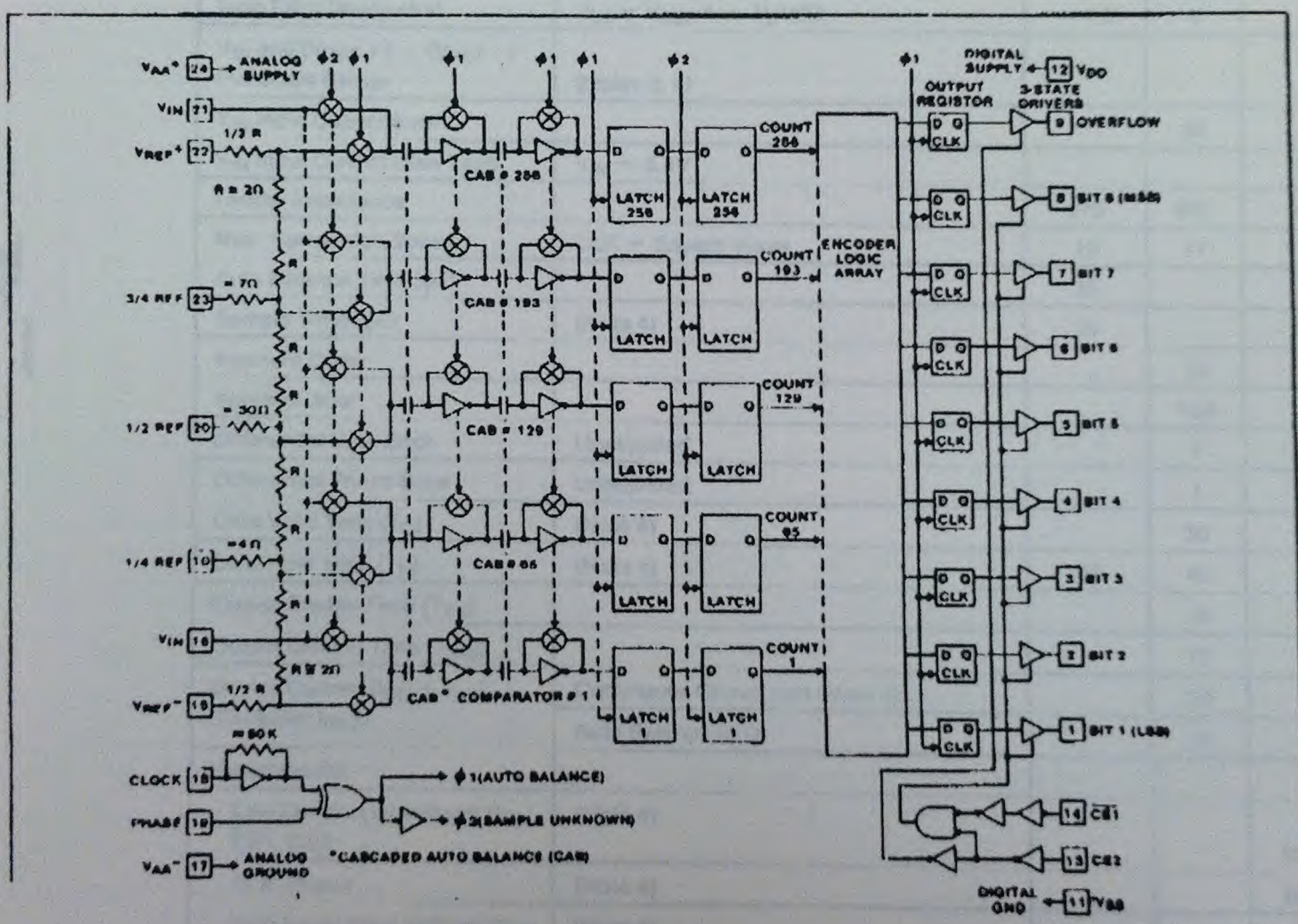
Lead Temperature (During Soldering)
At Distance 1/16 in. ± 1/32 in. (1.59 mm ± 0.79 mm) from Case for 10s Max ..... +265°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Voltage Range
(V_{DD} or V_{AA}^+) ..... 4V Min to 7.5V Max

Recommended V_{AA}^+ Operating Range ..... V_{DD} ±1V

Recommended V_{AA}^- Operating Range ..... V_{SS} ±1V



0194-2

Figure 2: Function Diagram

NOTE: All typical values have been characterized but are not tested.

CA3318C

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions at 25°C $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15 MHz, All Ref. Points Adjusted (Unless Otherwise Noted)	Limits			Units
		Min	Typ	Max	
Resolution		8			Bits
Integral Linearity Error				±1.5	LSB
Differential Linearity Error				+1, −0.8	LSB
Quantizing Error				±0.5	LSB
Maximum Input Bandwidth	(Note 1) CA3318C	2.5			MHz
Offset Error, Unadjusted	$V_{IN} = V_{REF}- + ½$ LSB	−0.5	4.5	6.4	LSB
Gain Error Unadjusted	$V_{IN} = V_{REF}+ - ½$ LSB	−1.5	0	1.5	LSB
V_{IN} and $(V_{REF}+) - (V_{REF}-)$ Full Scale Range	(Notes 2, 4)	4		7	V
V_{IN} Input Capacitance			30		pF
V_{IN} Input Current (See Text)	$V_{IN} = 6.4V$			3.5	mA
Ladder Impedance		270	500	800	Ω
Max. Conversion Speed	CLK = Square Wave	15	17		MSPS
Auto Balance Time (ϕ1)		33		∞	ns
Sample Time (ϕ2)	(Note 4)	25		500	ns
Aperture Delay			15		ns
Aperture Jitter			100		pS
Differential Gain Error	Unadjusted		2		%
Differential Phase Error	Unadjusted		1		%
Data Valid Time (T_D)	(Note 4)		50	65	ns
Data Hold Time (T_H)	(Note 4)	25	40		ns
Output Enable Time (T_{EN})			18		ns
Output Disable Time (T_{DIS})			18		ns
Device Current ($I_{DD} + I_{AA}$) (Excludes I_{REF})	Continuous Conversion (Note 4)		30	60	mA
	Auto Balance (ϕ1)		30	60	
Digital Inputs:					
Low Level Input Voltage V_{OL}: $\overline{CE1}$, CE2	(Note 4)			0.2 V_{DD}	V
CLK, Phase	(Note 4)			0.2 V_{AA}	V
High Level Input Voltage V_{IN}: $\overline{CE1}$, CE2	(Note 4)	0.7 V_{DD}			V
CLK, Phase	(Note 4)	0.7 V_{AA}			V
Input Leakage Current, I_I: Except CLK Input	(Note 3)		±0.2	±5	µA
Input Capacitance, C_I			3		pF

CA3318C

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions at 25°C $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15 MHz, All Ref. Points Adjusted (Unless Otherwise Noted)	Limits			Units
		Min	Typ	Max	
Digital Outputs:					
Output Low (Sink) Current	$V_O = 0.4V$	4	10		mA
Output High (Source) Current	$V_O = 4.5V$	−4	−6		mA
3-State Output Off-State Leakage Current, I_{OZ}			±0.2	±5	µA
Output Capacitance, C_O			4		pF

NOTE 1: A full scale sine wave input of greater than $F_{clock}/2$ or the specified input bandwidth (whichever is less) may cause an erroneous output code. The −3 dB bandwidth for frequency response purposes is greater than 30 MHz.

2. V_{IN} (Full Scale) or $V_{REF}+$ should not exceed $V_{AA}+ + 1.5V$ for accuracy.

3. The clock input is a CMOS inverter with a 50 kΩ feedback resistor and may be AC coupled with 1 V_{p-p} min. source.

4. Parameter not tested, but guaranteed by design or characterization.

Table 1: Pin Description

Pin	Name	Description
1	B1	Bit 1 (LSB)
2	B2	Bit 2
3	B3	Bit 3
4	B4	Bit 4
5	B5	Bit 5
6	B6	Bit 6
7	B7	Bit 7
8	B8	Bit 8 (MSB)
		Output Data Bits (High = True)
9	OF	Overflow
10	¼ R	Reference Ladder ¼ Point
11	V_{SS}	Digital Ground
12	V_{DD}	Digital Power Supply, +5V
13	CE2	Three-State Output Enable Input, Active Low. See Table 2.
14	$\overline{CE1}$	Three-State Output Enable Input, Active High. See Table 2.
15	$V_{REF}-$	Reference Voltage Negative Input
16	V_{IN}	Analog Signal Input
17	$V_{AA}-$	Analog Ground
18	CLK	Clock Input
19	PHASE	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).
20	½ R	Reference Ladder Midpoint
21	V_{IN}	Analog Signal Input
22	$V_{REF}+$	Reference Voltage Positive Input
23	¾ R	Reference Ladder ¾ Point
24	$V_{AA}+$	Analog Power Supply, +5V

Table 2: Chip Enable Truth Table

$\overline{CE1}$	CE2	B1–B8	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

DEVICE OPERATION

A sequential parallel technique is used by the CA3318 converter to obtain its high-speed operation. The sequence consists of the "Auto-Balance" phase, $\phi 1$, and the "Sample Unknown" phase, $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle*. With the phase control (pin 19) high, the "Auto-Balance" ($\phi 1$) occurs during the high period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

*This device requires only a single-phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the high and low periods of the same clock.

NOTE: All typical values have been characterized but are not tested.

CA3318C

During the "Auto-Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(N/256)\,V_{REF}] - (1/512)\,V_{REF}]$$
$$= [(2N-1)/512]\,V_{REF}$$

Where:

$V_{tap}(n)$ = reference ladder tap voltage at point n.

V_{REF} = voltage across $V_{REF}-$ to $V_{REF}+$

N = tap number (1 through 256)

The other side of these capacitors are connected to single-stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately $(V_{AA}+ - V_{AA}-)/2$. The first set of capacitors now charges to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers is also auto-balanced. The balancing of the second-stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{IN} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{IN} will go to a "high" state at their outputs. All comparators that had tap voltages lower than V_{IN} will go to a "low" state.

The status of all these comparator amplifiers is ac coupled through the second-stage comparator and stored at the end of this phase ($\phi 2$) by a latching amplifier stage. The latch feeds a second latching stage, triggered at the end of $\phi 1$. This delay allows comparators extra settling time. The status of the comparators is decoded by a 256 to 9-bit decoder array, and the results are clocked into a storage register at the end of the next $\phi 2$.

A 3-stage buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B8 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device, a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous-Clock Operation

One complete conversion cycle can be traced through the CA3318 via the following steps. (Refer to timing diagram.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the first-stage latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto-balance" phase for the comparators. During this "low" state of the clock, the output of the latches settles and is captured by a second row of latches when the clock returns high. The second-stage latch output propagates through the decode array, and a 9-bit code appears at the D inputs of the output registers. On the next falling edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the end of the next "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse-Mode Operation

The CA3318 needs two of the same polarity clock edges to complete a conversion cycle: If, for instance, a negative going clock edge ends sample "N", then data "N" will appear after the next negative going edge. Because of this requirement, and because there is a maximum sample time of 500 ns (due to capacitor droop), most pulse or intermittent sample applications will require double clock pulsing.

If an indefinite standby state is desired, standby should be in auto-balance, and the operation would be as in Figure 5A.

If the standby state is known to last less than 500ns and lowest average power is desired, then operation could be as in Figure 5B.

Increased Accuracy

In most cases the accuracy of the CA3318 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, five adjustments can be made to obtain better accuracy, i.e., offset trim; gain trim; and ¼, ½ and ¾ point trim.

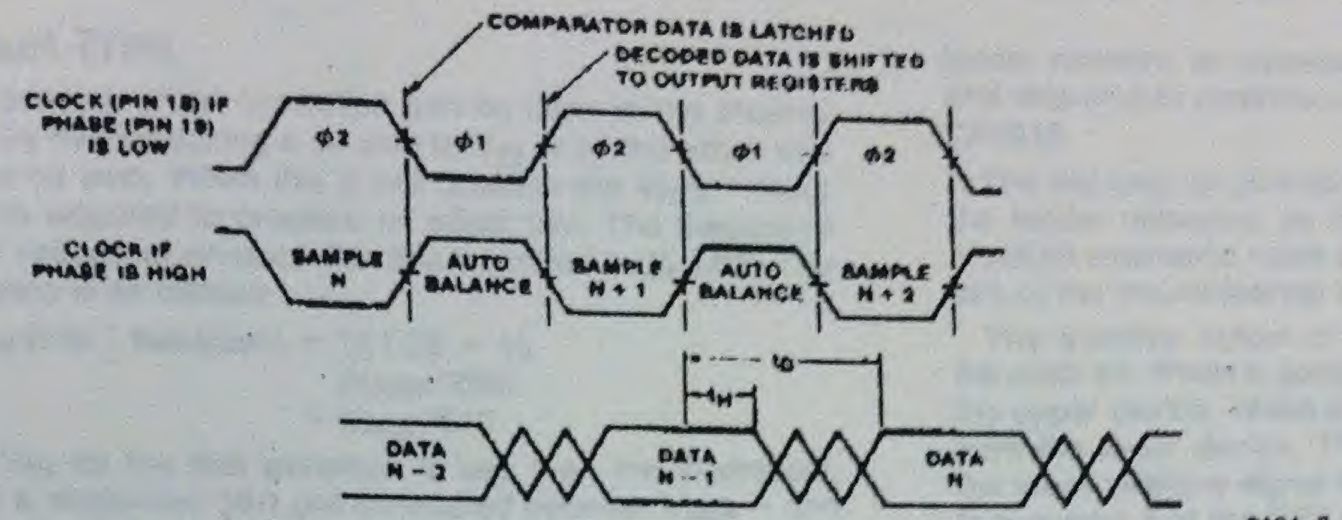


Figure 3: Input to Output Timing Diagram

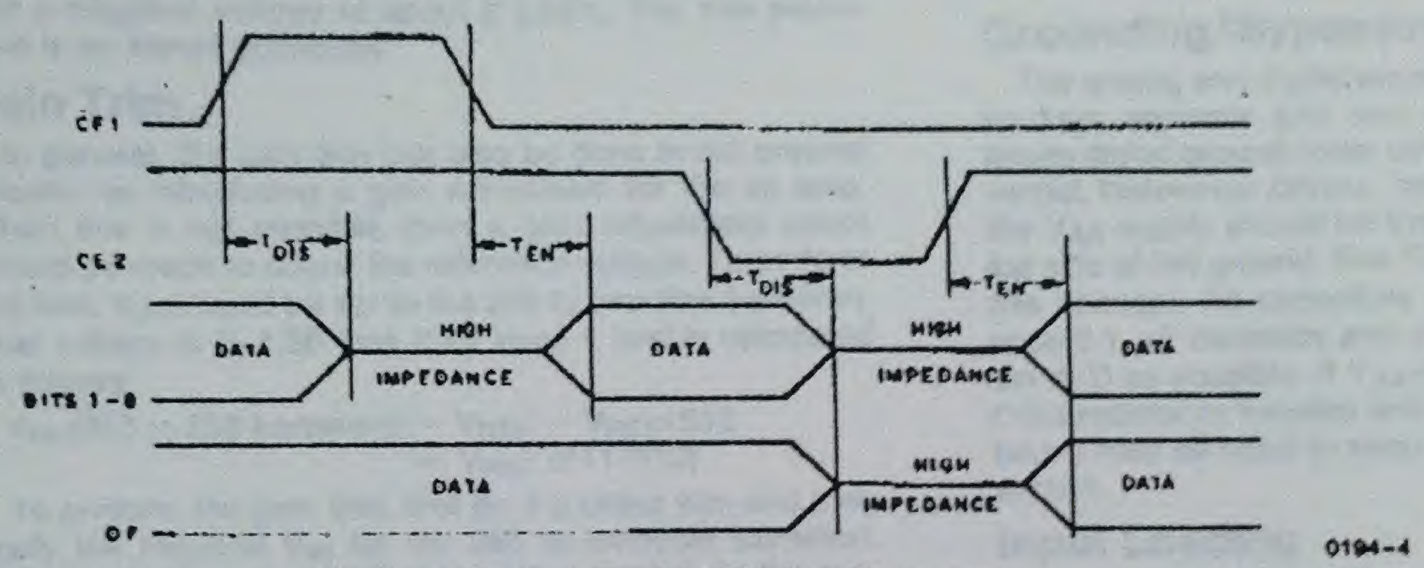
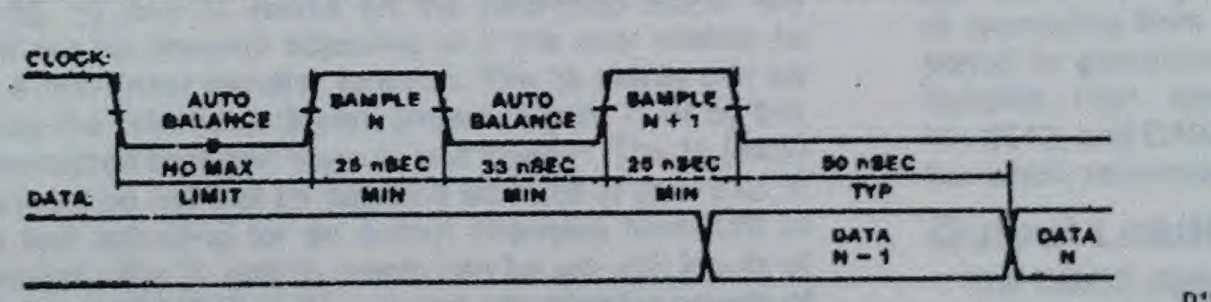
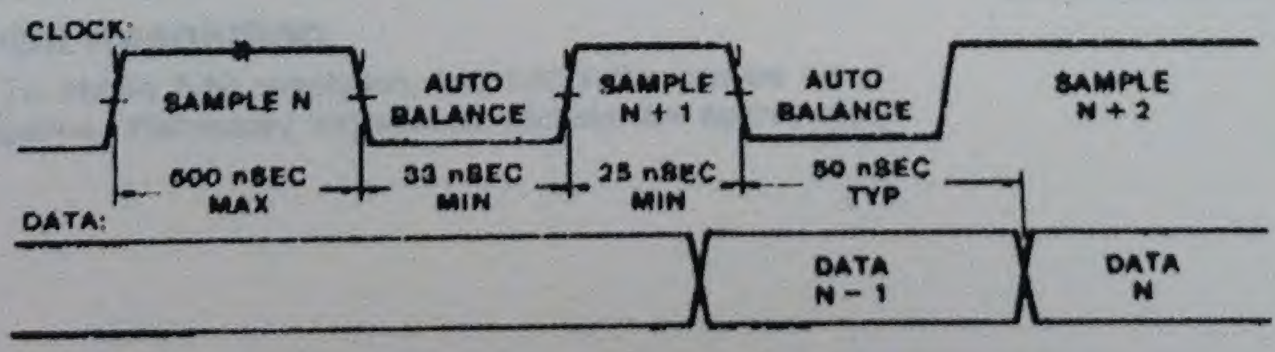


Figure 4: Output Enable Timing Diagram



A: Standby in Indefinite Auto Balance (Shown with Phase = Low)



B: Standby in Sample (Shown with Phase = Low)

Figure 5: Pulse Mode Operation

NOTE: All typical values have been characterized but are not tested.

5

Offset Trim

In general, offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the $V_{REF}-$ input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2} (V_{REF}/256) = V_{REF}/512$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between $V_{REF}-$ and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0-to-1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between $V_{REF}-$ and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general, the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 255 to overflow transition. That voltage is ½ LSB less than $V_{REF}+$ and is calculated as follows:

$$V_{IN} \text{ (255 to 256 transition)} = V_{REF} - V_{REF}/512 = V_{REF} (511/512)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 255 to overflow transition. Now adjust $V_{REF}+$ until that transition occurs on the outputs

¼ Point Trims

The ¼, ½ and ¾ points on the reference ladder are brought out for linearity adjusting or if the user wishes to create a non-linear transfer function. The ¼ points can be driven by the reference drivers shown (Figure 7) or by 2-K pots connected between $V_{REF}+$ and $V_{REF}-$. The ½ (mid-) point should be set first by applying an input of 257/512 × (V_{REF}) and adjusting for an output changing from 128 to 129. Similarly the ¼ and ¾ points can be set with inputs of 129/512 and 385/512 × (V_{REF}) and adjusting for counts of 192 to 193 and 64 to 65. (Note that the points are actually ¼, ½ and ¾ of full scale + 1 LSB.)

9-Bit Resolution

To obtain 9-bit resolution, two CA3318's can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls—all of which are available on the CA3318.

The first step for connecting a 9-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 8. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the ninth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 8) are now connected in parallel to complete the circuitry. The complete circuit for a 9-bit A/D converter is shown in Figure 9.

Grounding/Bypassing

The analog and digital supply grounds of a system should be kept separate and only connected at the A/D. This keeps digital ground noise out of the analog data to be converted. Reference drivers, input amps, reference taps, and the V_{AA} supply should be bypassed at the A/D to the analog side of the ground. See Figure 10 for a block diagram of this concept. All capacitors shown should be low impedance 0.1 µF ceramics and should be mounted as close to the A/D as possible. If $V_{AA}+$ is derived from V_{DD}, a small (10Ω resistor or inductor and additional filtering (4.7 µF tantalum) may be used to keep digital noise out of the analog system.

Input Loading

The CA3318 outputs a current pulse to the V_{IN} terminal at the start of every sample period. This is due to capacitor charging and switch feedthrough and varies with input voltage and sampling rate. The signal source must be capable of recovering from the pulse before the end of the sample period to guarantee a valid signal for the A/D to convert. Suitable high speed amplifiers include the HA-5033, HA 2542; and CA3450. Figure 11 is an example of an amplifier which recovers fast enough for sampling at 15 MHz.

Output Loading

The CMOS digital output stage, although capable of driving large loads, will reflect these loads into the local ground. It is recommended that a local QMOS buffer such as CD74HC541E be used to isolate capacitive loads.

Table 3: Output Code Table

Code Description	Input Voltage* V_{REF} 6.40V (V)	Input Voltage* V_{REF} 5.12V (V)	Binary Output Code OF	MSB B8	B7	B6	B5	B4	B3	B2	LSB B1	Decimal Count
Zero	0.00	0.00	0	0	0	0	0	0	0	0	0	0
1 LSB	0.025	0.02	0	0	0	0	0	0	0	0	1	1
2 LSB	0.05	0.04	0	0	0	0	0	0	0	1	0	2
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
¼ Full Scale	1.60	1.28	0	1	0	0	0	0	0	0	0	64
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
½ Full Scale - 1 LSB	3.175	2.54	0	0	1	1	1	1	1	1	1	127
½ Full Scale	3.20	2.56	0	1	0	0	0	0	0	0	0	128
½ Full Scale + 1 LSB	3.225	2.58	0	1	0	0	0	0	0	0	1	129
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
¾ Full Scale	4.80	3.84	0	1	1	0	0	0	0	0	0	192
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
Full Scale - 1 LSB	6.35	5.08	0	1	1	1	1	1	1	1	0	254
Full Scale	6.375	5.10	0	1	1	1	1	1	1	1	1	255
Over Flow	6.40	5.12	1	1	1	1	1	1	1	1	1	511

* The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

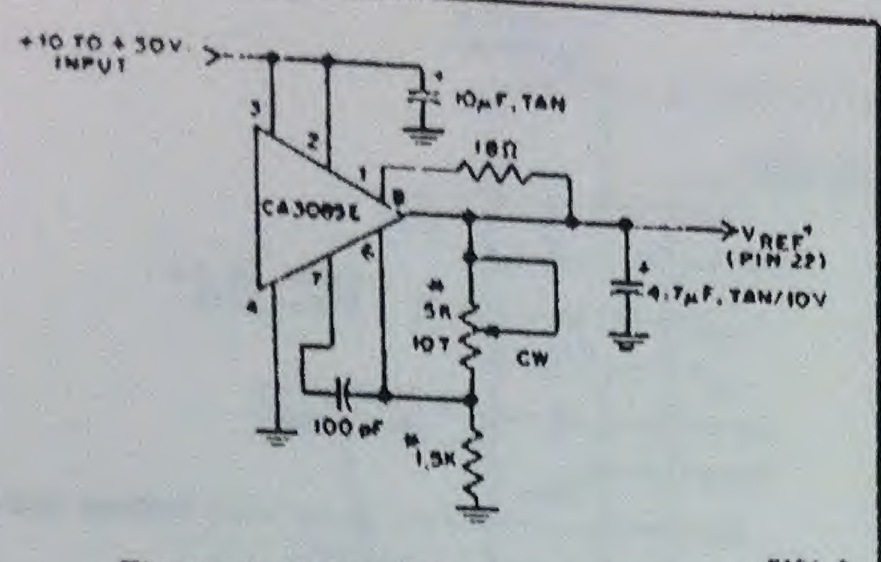
Reducing Power

Most power is consumed while in the auto-balance state. When operating at lower than 15 MHz clock speed, power can be reduced by stretching the sample ($\phi 2$) time. The constraints are a minimum balance time ($\phi 1$) of 33ns, and a maximum sample time of 500ns. Longer sample times cause droop in the auto-balance capacitors. Power can also be reduced in the reference string by switching the reference on only during auto-balance.

Clock Input

The Clock and Phase inputs feed buffers referenced to $V_{AA}+$ and $V_{AA}-$. Phase should be tied to one of these two potentials, while the clock (if DC coupled) should be driven at least from 0.2 to 0.7 $\times$ ($V_{AA}+ - V_{AA}-$). The clock may also be AC coupled with at least a 1 V_{p-p} swing. This allows TTL drive levels or 5V OMOS levels when $V_{AA}+$ is greater than 5V.

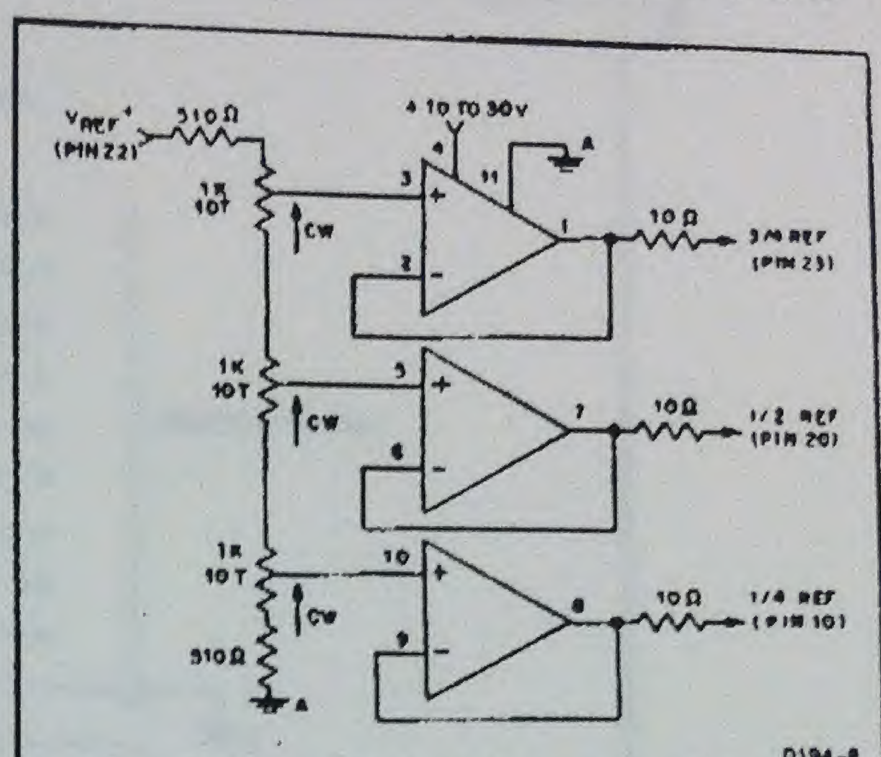
CA3318C



0104-7

Figure 6: Typical Voltage Reference Source for Driving $V_{REF}+$ Input

NOTE: Bypass $V_{REF}+$ to Analog Ground Near A/D with 0.1 μF Ceramic Cap. Parts Marked (*) Should Have Low Temperature Drift



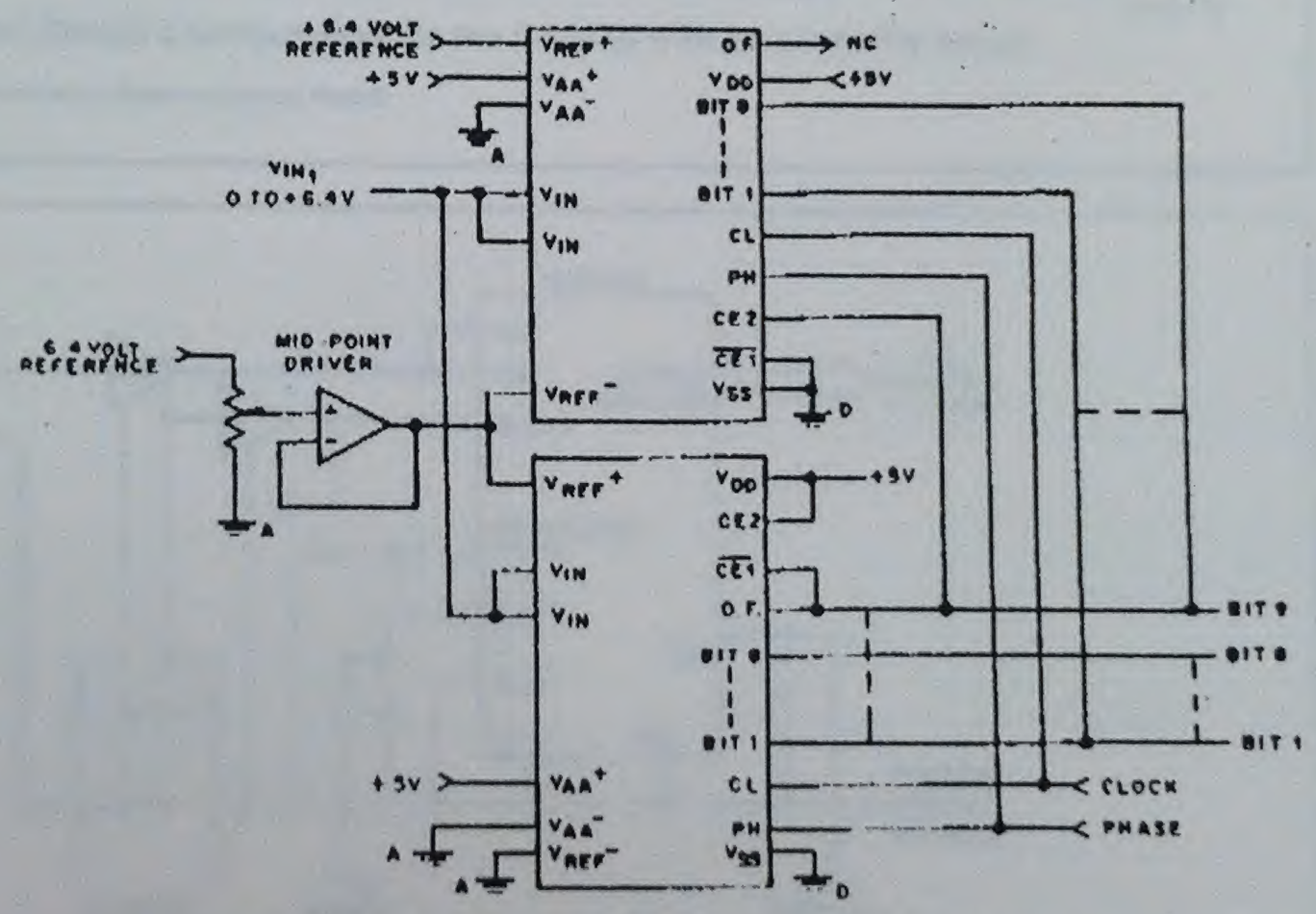
0194-8

Figure 7: Typical ¼ Point Drivers for Adjusting Linearity (Use for Maximum Linearity)

NOTE: All Op Amps = ¼ CA324E

Bypass All Reference Points to Analog Ground Near A/D with 0.1 μF Ceramic Caps

Adjust $V_{REF}+$ First, then ½, ¾ and ¼ Points.



0194-9

Figure 8: Using two CA3318's for 9-Bit Resolution

NOTE: Reference Taps and V_{AA} Should be Bypassed to AGND with 0.1 μF Low Impedance Caps.

The Mid-Point Driver must be Stable with Capacitive Loads.

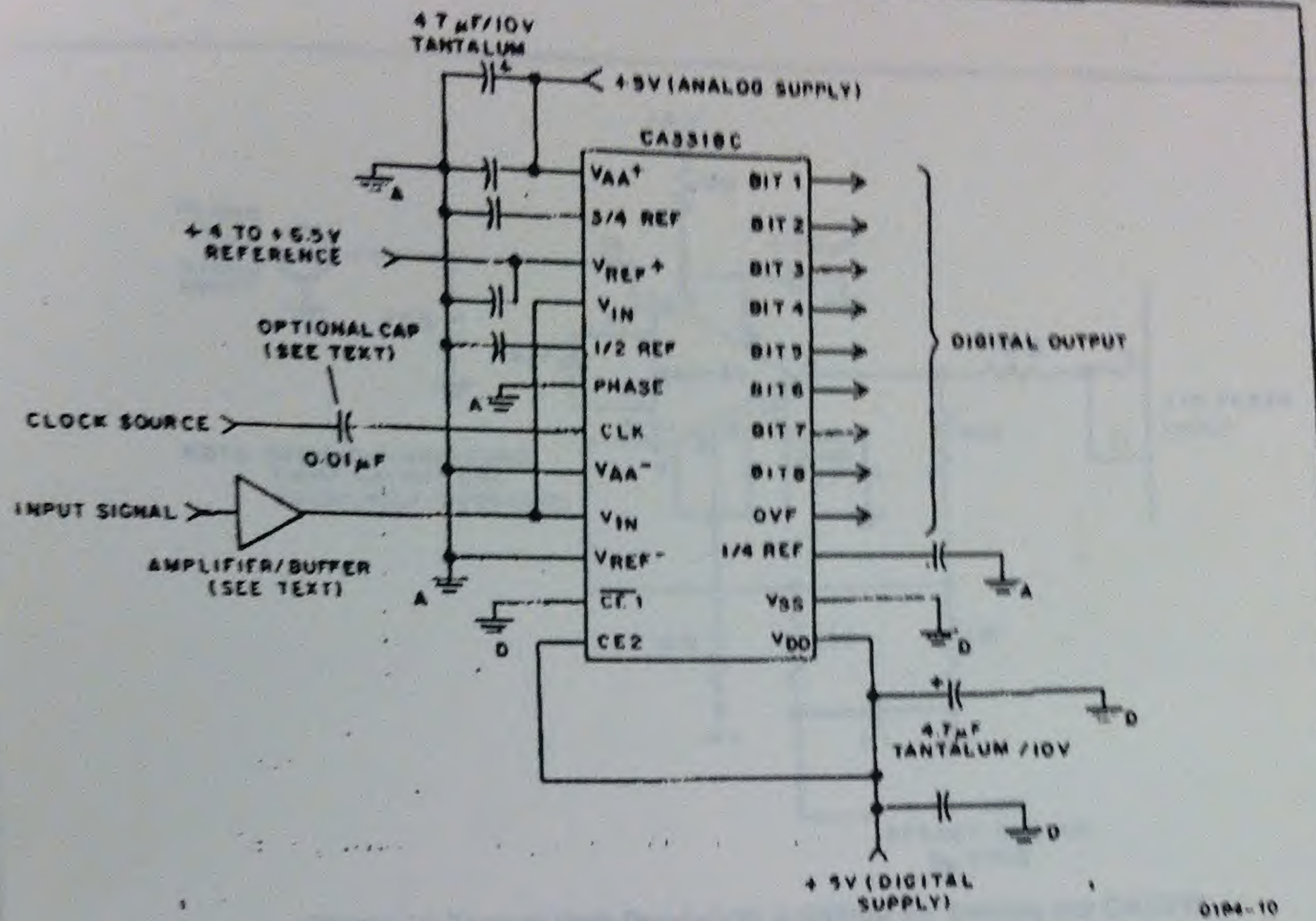


Figure 9: Typical Circuit Configuration for the CA3318 with No Linearity Adjust

NOTE: All Capacitors = 0.1 μF, Low Inductance Ceramic (Unless Noted)

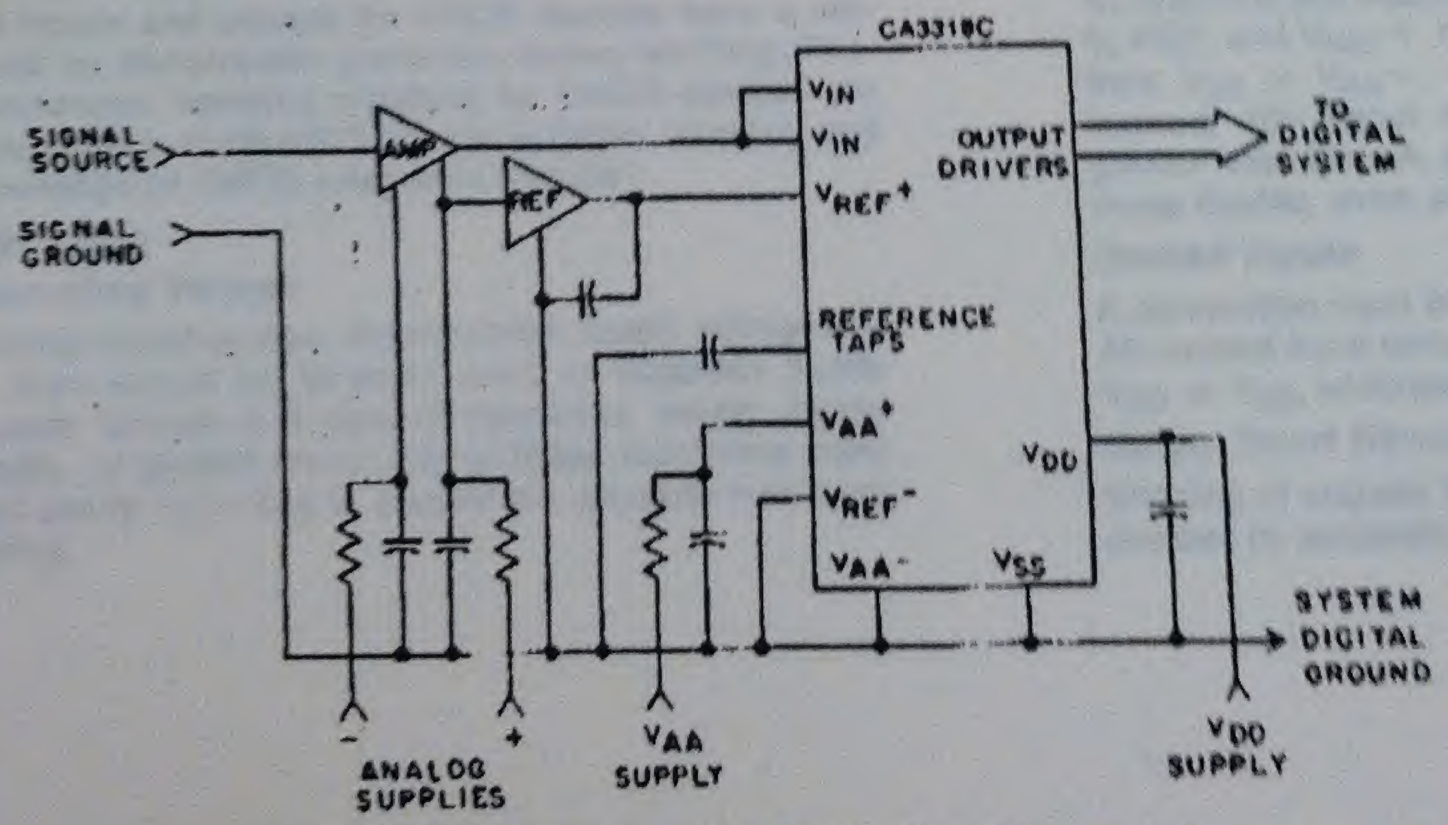


Figure 10: Typical System Grounding/Bypassing

NOTE: All typical values have been characterized but are not tested.

CA3318C

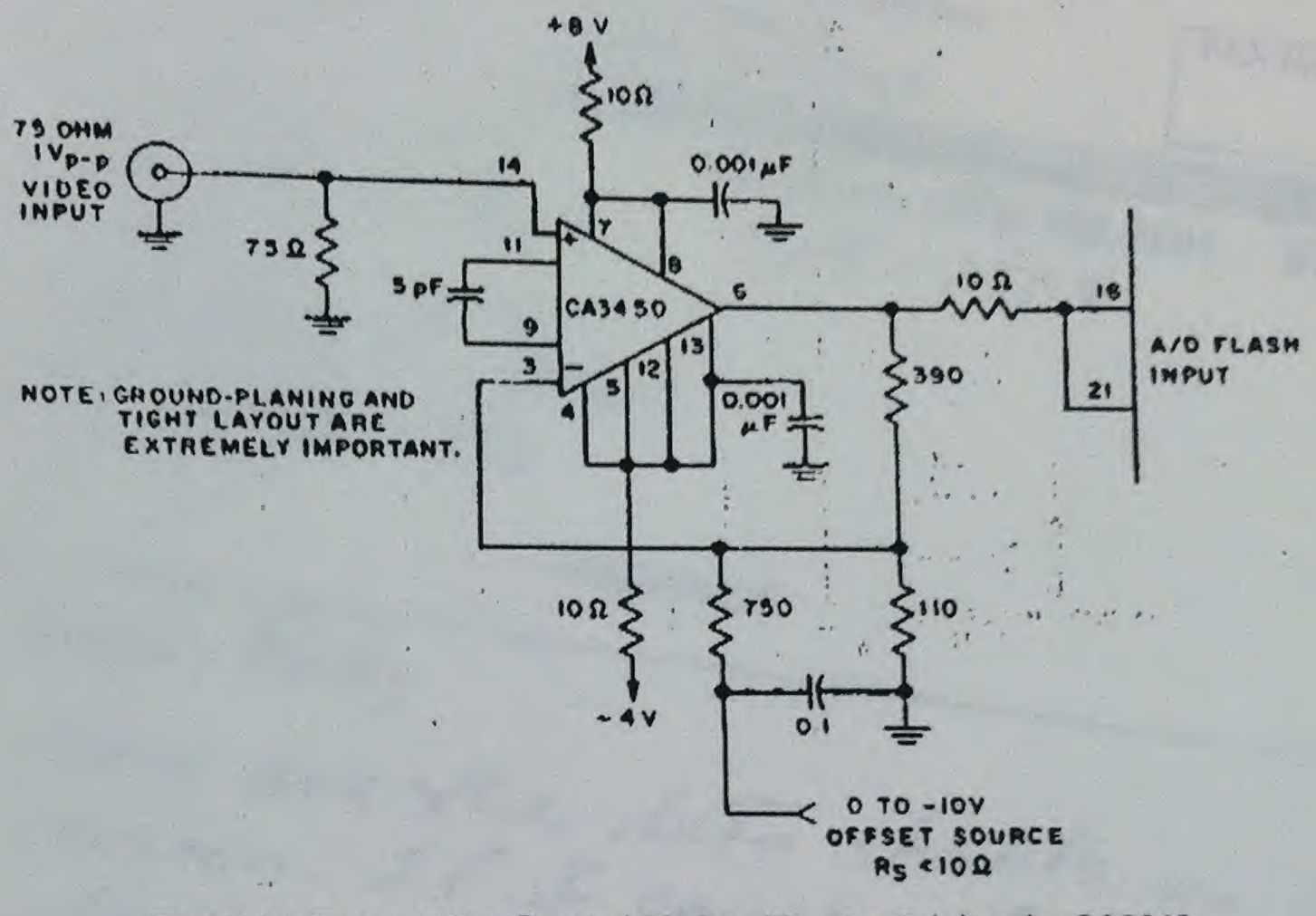


Figure 11: Typical High Bandwidth Amplifier for Driving the CA3318

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**

   All inputs and outputs for CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. **Operating**

   Operating Voltage

   During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

   Input Signals

   As shown in the maximum ratings, all inputs except V_{In}, ¾ REF, and $V_{REF}+$ have diodes to V_{DD} or $V_{AA}+$ and from V_{SS} or $V_{AA}-$. V_{In}, ¾ REF, and $V_{REF}+$ have, instead, 10V zener diodes to $V_{AA}-$. No current of greater than 20 mA should be allowed through any of these diodes, even when the supplies are off.

   Unused Inputs

   A connection must be provided at every input terminal All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

   Output Short Circuits

   Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.